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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,232	12/27/2001	Leo Temoshenko	062891.0662	9099

5073 7590 04/07/2006

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EXAMINER	
CHUNG, JI YONG DAVID	
ART UNIT	**PAPER NUMBER**
2143	

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,232	TEMOSHENKO ET AL.	
	Examiner	Art Unit	
	Ji-Yong D. Chung	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/12/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

Response to Remarks

1. Applicant's arguments and amendments filed on January 12, 2006 have been carefully considered but they are deemed moot in light of new grounds of rejection.

The prior rejections have been withdrawn in light of the amendment.

In the instant amendment, the applicant has overcome the prior art of record (Jungck et al.) cited as the basis of the Office's rejections, as provided in the second, Final Office action. The Office has conducted an additional search, in hope that the search will ensure the validity of a patent, if granted, to the applicant. Unfortunately, the Office has discovered an additional prior art reference that pertains to the instant application. Specifically, the reference at issue is Muller et al. (Pat. No: &S 6,453,360).

The Office is compelled to raise substantive issues, as set forth below.

While Muller shows many features on which the current independent claims maybe viewed to read, the Office believes that minor changes in language of the claims should place the claims in condition to overcome the rejections or to resolve any issues that are raised below.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-5, 11-12, 16-18, and 21-22** are rejected under 35 U.S.C. 103(a) as being anticipated by Muller et al. (Pat. No.: US 6,453,360, Muller hereinafter)

With regard to **claim 1**, Muller shows:

a gateway [See lines 5-13 in column 13 and lines 50-54 in column 8] *for processing packets in a multi-processor environment, comprises*:

a line interface operable to receive a set-up request packet [See Fig. 1A. The request packet is the first packet enters the process in Fig. 7. See from line 53 in column 50 to line 53 in column 53 for explanation of Fig. 7. The 'Load Distributor' and 'input processing module' are the line interface. See Fig. 1A for how input processing module receives packets. See lines 8-18 in column 10];

a switch processor operable to process set-up request packet [Flow Database manager and header parser in Fig. 1A are the 'switch processor.' The header parser generates flow keys, which designates one of many processors on the multi-processor host. The header parser processes 'request packet' as well as all other packets. See lines 1-14 in column 13];

a plurality of processors, the switch processor operable to direct the set-up request packet to a selected one of the plurality of processors [See lines 52-61 in column 49. The processors are located on the 'host.' (They can also be located on the NIC. See lines 58-61 in column 49)];

the selected one of the plurality of processors operable to generate a set-up reply packet in response to the set-up request packet [A router or a gateway has the ability to produce a packet (which maybe dubbed a "reply" packet. It is not shown that, a packet would be produced by the host processor, however], *the set-up reply packet including a virtual identifier associated with the selected one of the plurality of processors as assigned by the switch processor* [All packets in the system contain header information ("virtual identifier") which results in the generation of flow keys (See lines 27-35 in column 18. Based on the generated flow key, a processor is assigned (See lines 36-41, column 18], *the selected one of the plurality of processors operable to transport the set-up reply packet through the line interface in order to establish communication session with the selected one of the plurality of processors* [In a routing gateway, any packet processed or generated in the gateway must leave through the NIC shown in Fig. 1A. That is, a packet arrives through the NIC to a selected host processor for the packet; if the packet is processed (e.g., header rewritten), it becomes a "response packet") or responded to (and thus generating a "response packet"), it must leave through the NIC], *the line interface operable to route subsequent packets associated with the communication session directly to the selected one of the plurality of processors in response to the virtual identifier without requiring initial processing by the switch processor.* Once flow data, along with the flow key, are stored by the flow database manager (part of "switch processor"), there is no need to further store another flow for the same "session."

With regard to **claim 2**, Muller shows *the line interface is operable to receive an information request packet in the communication session, the information request packet*

including the virtual identifier, the line interface operable to direct the information request packet to the selected one the plurality of processors associated with the virtual identifier. Any subsequent packets that arrive after the first packet in the flow are "information request packets." These are directed to one of the host processors.

With regard to **claim 3**, Muller shows *the selected one of the plurality of processors is operable to generate an information reply packet in response to the information request packet, the information reply packet including the virtual identifier* [As indicated in the discussion of all packets (response or reply) in the described system contains information for generating flow keys. This information in the header is "virtual identifier." See also lines 32-47 in column 10. All packets contains source and destination addresses.]

With regard to **claim 4**, Muller shows *a virtual identification manager, the virtual identification manager comprising one or more associations of one or more virtual identifiers with one or more of the plurality of processor.* Earlier, it was indicated that a flow key identifies a flow. In addition, the flow key also identifies a processor by mapping or hashing. See lines 49-52 in column 50. See Flow Database 110 for "virtual identification manager." See Flow Database, which contains flow keys ("associations of one or more virtual identifiers with one or more of the plurality of processors").

With regard to **claim 5**, Muller shows *the switch processor is operable to designate the associations between virtual identifiers and the plurality of processors to the line interface.* In

Mullen, the header parser (part of the line switch processor) is operable to produce a flow key (see the discussion of claim 1) and thus "designate" the associations between the virtual identifiers and the plurality of processors, by producing flow keys. Each flow key is submitted to the line interface ('load distributor', which is part of "the switch processor").

Claims 12, 18, and 22 substantively refer to the limitation "identifying the virtual identifier" in various forms of claim language. The header parser performs the function.

Claims 11-12, 16-18, and 21-22 substantively incorporate a number of limitations from the set of all limitations of claims 1-5, but in method form, means-plus-function form, and in software product form, rather than in apparatus form. The reasons for the rejections of claims 1-5 apply to claims 11-12, 16-18, and 21-22. Therefore, claims 11-12, 16-18, and 21-22 are rejected for substantially the same reasons.

4. **Claim 6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller in view of Ayanoglu (Pat. No. 5,717,689).

With regard to **claim 6,** Muller does not show, but Ayanoglu shows *switching fabric operable to route packets to the plurality of processors, the line interface operable to provide information packets received in the communication session to the switching fabric for routing to the selected one of the plurality of processors without directly engaging the switch processor.* See Fig. 4, and see lines 41-64 in column 4.

It would have been obvious to one of ordinary skill in the art at the time of the invention to place a switching fabric between the processors and the interface, as shown by Ayanoglu, because the switching fabric would increase the speed of data transport.

5. **Claims 7-9, 13-14, 19, and 23-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller in view of Kap (Pat. No. 4,941,087).

In reference to **claim 7**, Muller does not show, but Kap shows *the switch processor* [See lines 13-29 in column 8 for CUS and SCU (a central unit selector and synchronization control unit)] *selects a backup processor addition to the selected one of the plurality of processors* [See Fig. 4 for backup processors and primary processors ("plurality of processors")], *the backup processor operable to process the communication session in response to a failure in the selected one of the plurality of processors*. [Kap shows a system in which a failed processor replaces the primary processor].

It would have been obvious to to one of ordinary skill in the art at the time of the invention to adapt Kap's system to provide for a backup processor, with the switching processor controlling the processor selection, because the adapting Kap's system to Muller would provide for failover.

In reference to **claim 8**, Kap and Muller would be combined so that *the backup processor is assigned selected one of the virtual identifiers*. The selected processor would process a

particular set of packets; this would be assigned. The backup would have, by default, been assigned the same set of packets and the same flow keys.

In reference to **claim 9**, Kap shows *the switch processor provides state information to the backup processor, the state information associated with the communication session associated with the selected one of the plurality of processors.* SCU writes down the important operation of the primary unit, so that, upon failure, the backup processor can resume from the point of failure. See lines 50-55 in column 8.

Claims 13 and 23 substantively incorporate all the limitations of claims 7-9, but in method form and software product form, rather than in apparatus form. The reasons for the rejections of claims 7-9 apply to claims 13 and 23. Therefore, claims 13 and 23 are rejected for substantially the same reasons.

In reference to **claims 14, 19, and 24**, the substance of all their limitations, except two, have been discussed. The discussion of the two limitations follows, with reference to claim 14. Claims 19 and 24 incorporate the two limitations in means-plus-function form and in software product form, rather than in method form. Therefore, the following discussion also applies to claims 19 and 24.

In **claim 14**, the two limitations are:

determining whether the selected one of the plurality of processors associated with the virtual identifier is operational [See lines 56-68 in column 11. Occurrence of an error determines whether the selected one of the processors is operational]; and

directing the data packet to the backup processor in response to the selected one of the plurality of processors associated with the virtual identifier not being operational [This feature is not explicitly stated. However, as indicated in the preceding discussions, the primary and the backup handle the same flow keys. Thus, upon the failure of the primary processor and upon the backup processor taking over its role, the packets that were directed to the original primary processor would be directed to the backup processor after the failure.].

6. **Claim 10, 15, 20, and 25** is rejected under 35 U.S.C. 103(a) as being unpatentable over Muller in view of Isfeld et al. (Pat. No. 5,802,278, Isfeld hereinafter).

With regard to **claim 10**, Muller does not show, but Isfeld shows *the plurality of processors are operable to query the switch processor* for an associated virtual identifier upon *initialization.* See Fig. 24 for DPM ("processors"). See lines 15-34 in column 41. The

It would have been obvious to one of ordinary skill in the art at the time of the invention to have one of the "plurality of processors" shown in Muller (after initialization), because Isfeld shows that one of the plurality of the processors can query the central processor ("switching processor") for more information on the packets.

Claims 15, 20, and 25 substantively incorporate all the limitations of claim 10, but in method form, means-plus function form, and software product form, rather than in apparatus form. The reasons for the rejections of claim 10 apply to claims 15, 20, and 25. Therefore, claims 15, 20, and 25 are rejected for substantially the same reasons.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ji-Yong D. Chung whose telephone number is (571) 272-7988. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ji-Yong D. Chung
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Art Unit: 2143

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